UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,815	10/08/2003	Wayne Dervon Kever	100204840-1	6616

22879 7590 08/05/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
LIN, SUN J	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	**Application No.** 10/681,815	**Applicant(s)** KEVER ET AL.	
	Examiner Sun J. Lin	**Art Unit** 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/08/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/681,815 filed on 10/08/2003. Claims 1 – 18 remain pending in the application.

Specification Objections

2. The specification is objected to because of following informalities:

Page 6, Paragraph 0031, line 7, change "X1" to —**X2**—.
Page 6, Paragraph 0032, line 7, change "172" to —**272**—.
Page 7, Paragraph 0035, line 2, before "circuit" insert —**second**—.
Page 7, Paragraph 0035, line 6, before "circuit" insert —**second**—.

Appropriate correction is required.

Drawing Objections

3. Drawings are objected to because of following informalities:

Figure 1, change "ORIGINAL LAYOUT 120" to —**FIRST LAYOUT 120**—.
Figure 4, below box labeled "278" insert —**W2**—.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 4 and 6 – 17 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 5,936,868 to *Hall*.

6. As to Claim 1, *Hall* shows and discloses the following subject matter:

- A process for downward size scaling (i.e., shrinking) of a layout for a VLSI using _different scaling factors_ (i.e., _asymmetrically shrinking_) – [col. 10, line 33; col. 3, line 39 – 53]; converting gate array cells to follow _new design rules_ requiring _non-uniform transformation_ (e.g., _asymmetrically shrinking_) of circuit components – [col. 2, line 1 – 14];
- Converting an _original IC design_ (i.e., _first VLSI circuit design layout_) defined by an _original manufacturing process_ (i.e., _first fabrication process_) to an _updated IC design_ (i.e., _second VLSI circuit design layout_) defined by an _updated manufacturing process_ (i.e., _second fabrication process_) – [col. 3, line 32 – 38]; _upgraded (i.e., updated) manufacturing process_ utilizes _tighter design rules_ – [col. 6, line 32 – 33]; Noted that the _original manufacturing process_ (_first fabrication process_) utilizes design rules, which are less tighter than that utilized by the _updated manufacturing process_ (_second fabrication process_);;
- Processing layouts of (transistor) cells (i.e., leaf cells) of the upgraded IC layout (second VLSI circuit design layout) to ensure conformity to the _tighter design rules_ (_second design rules_) – [col. 6, line 29 – 54].

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

7. As to Claims 8 and 15, reasons are included in **[Response A]** given above.

8. As to Claim 16, reasons are included in **[Response A]** given above. Noted that the updated manufacture process is performed by a layout update toll.

9. As to Claims 2 and 9, in addition reasons included in **[Response A]** given above, _Hall_ discloses _repositioning_ (i.e., _reorienting_) (transistor) cells in accordance with the _tighter design rules_ (_second design rules_) – [col. 29 – 42]. MOS transistor – [col. 8, line 8].

10. As to Claims 3 and 10, in addition reasons included in **[Response A]** given above, _Hall_ teaches performing first downward size scaling (with the same scaling factor) on

the mask data to scale down the (entire) *original IC design* – [col. 3, line 50 – 52]. Noted that, when scaling downward with the same scaling factor, all port instances within the original IC design (first VLSI circuit design layout) are maintained in the updated IC design (second VLSI circuit design layout).

For reference purposes, the explanations given above in response to Claims 3 and 10 are called **[Response B]** hereinafter.

11. As to Claims 4 and 11, in addition reasons included in [Response A] given above, Hall teaches processing vias (i.e., via arrays) of the updated IC design to conform to the second design rules – [col. 4, line 9 – 14].

12. As to Claims 6 and 13, reasons are included in **[Response A]** and **[Response B]**. Noted that when scaling downward with the same scaling factor, all design elements in the original IC design (first VLSI circuit design layout) are symmetrically scaled downward according the tighter second design rules.

13. As to Claims 7, 14 and 17, in addition reasons included in **[Response A]** and **[Response B]** given above, Hall teaches the following subject matter:

- Performing *first downward size scaling* (i.e., *symmetrical scaling*) on the *entire original IC design* (first VLSI design layout), including all port instances, for (update manufacturing process) – [col. 3, line 49 – 52];
- *Selectively* performing *second downward size scaling* (i.e., *asymmetric scaling*) to further scale down *contacts* for (updated manufacturing process) – [col. 3, line 52 – 53];
- *Selectively* performing *third downward size scaling* (i.e., *asymmetric scaling*) to further scale down *vias* for (updated manufacturing process) – [col. 3, line 52 – 53].

Noted that the *second and third downward size scaling* are asymmetric *scaling processes*, which only change the sizes of contacts and vias; therefore, locations of port instances are maintained relative to the asymmetric scaling between the original IC design (first VLSI circuit design layout) and the updated IC design (second VLSI circuit design layout).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. Claims 5, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,936,868 to *Hall* in view of U.S. Patent No. 6,756,242 to *Regan*.

16. As to Claim 5, *Hall* shows and discloses all subject matter as recited in Claim 1, he does not teach a process of verifying hierarchy associated with the updated IC design (second VLSI circuit design layout). But *Regan* shows *design hierarchy* of a circuit layout and teaches a process of verifying hierarchy design after modifying the design layout using a scaling factor – [Fig. 1; Fig. 20; abstract]. *Regan* teaches performing *verification of hierarchy* process on modifying (i.e., downsized) integrated circuit layout in order not to destroy the hierarchy of the circuit thereby maintaining its original functionality.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Regan* in performing *verification of hierarchy* process after modifying sizes of the original IC layout in order not to destroy the hierarchy of the original IC design thereby maintaining original functionality in the updated IC design.

For reference purposes, the explanations given above in response to Claim 5 are called **[Response C]** hereinafter.

17. As to Claims 12 and 18, reasons are included in **[Response C]** given above.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
August 4, 2005